What is claimed is:

1. A memory device, comprising:

a plurality of data output circuits, respective ones of which are configured to receive data from respective internal data lines and respective ones of which are coupled to respective data input/output pins; and

a data output control circuit operative to selectively enable subsets of the plurality of data output circuits to drive their respective corresponding data input/output pins responsive to an externally-applied control signal.

2. A memory device according to Claim 1, wherein the data output control circuit is operative to selectively cause subsets of the plurality of data output circuits to present a high impedance at their respective corresponding data input/output pins.

3. A memory device according to Claim 1, wherein the data output control circuit comprises:

a command decoder operative to generate test mode command signals and read command signals responsive to first externally-applied control signals; and

a data output selection circuit coupled to the command decoder and operative to selectively enable subsets of the plurality of data output circuits responsive to the test mode command signals, the read command signals, and second externally-supplied control signals.

4. A memory device according to Claim 3:

wherein the data output selection circuit comprises:

a data output controller circuit configured to receive a plurality of group control signals and operative to generate respective output control signals responsive to respective ones of the group control signals; and

a plurality of write inhibit signal input buffer circuits, respective ones of which are configured to receive respective ones of a plurality of externally-applied write inhibit signals and operative to generate respective ones of the group control signals therefrom; and

wherein respective subsets of the plurality of data output circuits are configured to receive respective ones of the output control signals and are operative to be enabled and disabled responsive thereto.

5. A memory device according to Claim 4, wherein the data output controller circuit comprises:

a first data output controller circuit that applies an enable signal to all of the plurality of data output circuits responsive to a read command signal generated by the command decoder;

a second data output controller circuit that receives a first group control signal and that generates a first group enable signal for a first subset of the plurality of data output circuits; and

a third data output controller circuit that receives a second group control signal and that generates a second group enable signal for a second subset of the plurality of data output circuits.

6. A memory device according to Claim 4, wherein the data output control circuit further comprises an write inhibit signal input buffer control circuit operative to enable the plurality of write inhibit signal input buffer circuits responsive to a test mode command signal generated by the command decoder.

7. A memory device according to Claim 6, wherein the write inhibit signal buffer control circuit further comprises:

a control signal generator circuit which outputs a write inhibit signal buffer control signal in response to a data write command signal from the command decoder; and

a logic circuit that logically combines the write inhibit signal buffer control signal and the test mode signal and responsively applies a write inhibit signal buffer enable signal to the plurality of write inhibit signal input buffer circuits.

8. A memory device according to Claim 7, wherein a write inhibit signal input buffer circuit of the plurality of write inhibit signal input buffer circuits comprises:

a voltage comparison circuit which, in response to first state of a first write inhibit buffer enable signal, compares a write inhibit signal to a reference voltage and outputs a first group control signal responsive to the comparison; and

an output control circuit, which, in response to a second state of the first write inhibit signal buffer control signal, forces the first group control signal to a signal ground voltage.

9. A memory device according to Claim 4, wherein a data output circuit of the plurality of data output circuits comprises:

a data input/output (DQ) buffer circuit configured to receive data from an internal data line and a output control signal from the data output controller circuit and operative to generate a synchronized data signal synchronized to the external clock signal in response thereto; and

a driver circuit that drives an input/output pin responsive to the synchronized data signal.

10. A memory device according to Claim 1, configured to operate as a double date rate synchronous dynamic random access memory (DDR SDRAM) .

11. A method of testing a memory device comprising a plurality of data output circuits, respective ones of which are configured to receive data from respective internal data lines and respective ones of which are coupled to respective data input/output pins of the memory device, the method comprising:

applying a control signal to the memory device to selectively enable a subset of the plurality of data output circuits to drive a load at their respective corresponding data input/output pins.

12. A method according to Claim 11, further comprising:

connecting data input/output pins coupled to first and second data output circuits of respective first and second subsets of the plurality of data output circuits in common to an external data line; and

alternately enabling the first and second data output circuits responsive to the control signal to drive the external data line with data from first and second different internal data lines of the memory device.

13. A method according to Claim 12, wherein the first data output circuit presents a high impedance to the external data line when the second data output circuit is enabled.

14. A method according to Claim 12, wherein alternately enabling the first and second data output circuits responsive to the control signal to drive the external data line with data from first and second different internal data lines of the memory device comprises:

generating a test mode command signal from a command decoder of the memory device;

enabling a plurality of write inhibit signal input buffers of the memory device responsive to the test mode command signal;

generating a first read command signal from the command decoder;

transitioning a first write inhibit signal at an input of a first write inhibit buffer of the memory device;

enabling the first subset of the plurality of data output circuits responsive to the first read command signal and to the transition of the first write inhibit signal to thereby drive a set of external data lines with data from a first set of internal data lines;

generating a second read command signal from the command decoder;

transitioning a second write inhibit signal at an input of a second write inhibit buffer;

enabling the second subset of the plurality of data output circuits responsive to the second read command signal and to the transition of the second write inhibit signal to thereby drive the set of external data lines with data from a second set of internal data lines.